PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Derderian et al.

Patent No.: 6,940,181 B2

Issued: September 6, 2005

For: THINNED, STRENGTHENED SEMICONDUCTOR SUBSTRATES AND PACKAGES INCLUDING SAME

Attorney Docket No.: 2269-5713US

VIA ELECTRONIC FILING

September 5, 2007

REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT FOR APPLICANTS' MISTAKES (37 C.F.R. § 1.323) AND PATENT OFFICE MISTAKES (37 C.F.R. § 1.322)

Attn.: Certificate of Corrections Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

It is noted that a combination of Applicant and Patent Office errors appear in this patent of a typographical nature or character and correction thereof does not involve such changes in the patent as would constitute new matter or would require reexamination. A certificate of correction in the form attached hereto is requested.

Please note that an Amendment Pursuant to 37 C.F.R. § 1.312(a) (copy enclosed) was filed concurrently with the issue fee on June 30, 2005, but the amendments contained therein were apparently not completely included in the printed patent. Attached is a copy of the previously filed Amendment Pursuant to 37 C.F.R. § 1.312(a) and the date-stamped postcard, acknowledging receipt by the PTO, to provide proof of such filing.

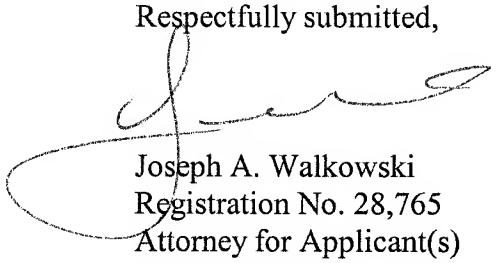
Please send the Certificate to:

Name: Joseph A. Walkowski
Address: TraskBritt
P.O. Box 2550
Salt Lake City, Utah 84110

The Commissioner is authorized to charge $100.00 to the TraskBritt Deposit Account No. 20-1469 for the fee as required by 37 C.F.R. § 1.20(a).

Attached hereto is Form PTO/SB/44, which is suitable for printing.

Respectfully submitted,



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Date: September 5, 2007
JAW/csw

Attachments: PTO/SB/44
copy of Amendment Pursuant to 37 C.F.R. § 1.312(a)
copy of date-stamped postcard

Document in ProLaw

PTO/SB/44 (08-07)
Approved for use through 08/31/2007. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : 6,940,181 B2
APPLICATION NO.: 10/690,339
ISSUE DATE : September 6, 2005
INVENTOR(S) : James M. Derderian and Nathan R. Draney

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the title page:
In ITEM (57), **ABSTRACT**,
8th line, change "enhance" to --enhances-- and change "provide" to --provides--

In the drawings:
In FIG. 9, change first line of label within the box identified by reference numeral 78 from "APPLY STRENGTHENING LAYER TO BACKSIDE" to--APPLY STRENGTHENING LAYER TO BACK SIDE--

In the specification:

COLUMN 3,	LINE 53,	change "packaging (act **122**) in" to --packaging in--
COLUMN 5,	LINE 29,	change "bonds conductive " to --bonds, conductive--
COLUMN 10,	LINE 53,	change "final back" to --final thinned back--
COLUMN 11,	LINE 6,	change "encapsulant." to --encapsulant **52**.--
COLUMN 11,	LINE 22,	after "FIGS. **4—6**," delete "and **6**"

MAILING ADDRESS OF SENDER (Please do not use customer number below):

Joseph A. Walkowski
TRASKBRITT
230 South 500 East, Suite 300
Salt Lake City, Utah 84102 USA

PTO/SB/44 (08-07)
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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : 6,940,181 B2
APPLICATION NO.: 10/690,339
ISSUE DATE : September 6, 2005
INVENTOR(S) : James M. Derderian and Nathan R. Draney

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Replace FIG. 9 with the following amended figure:

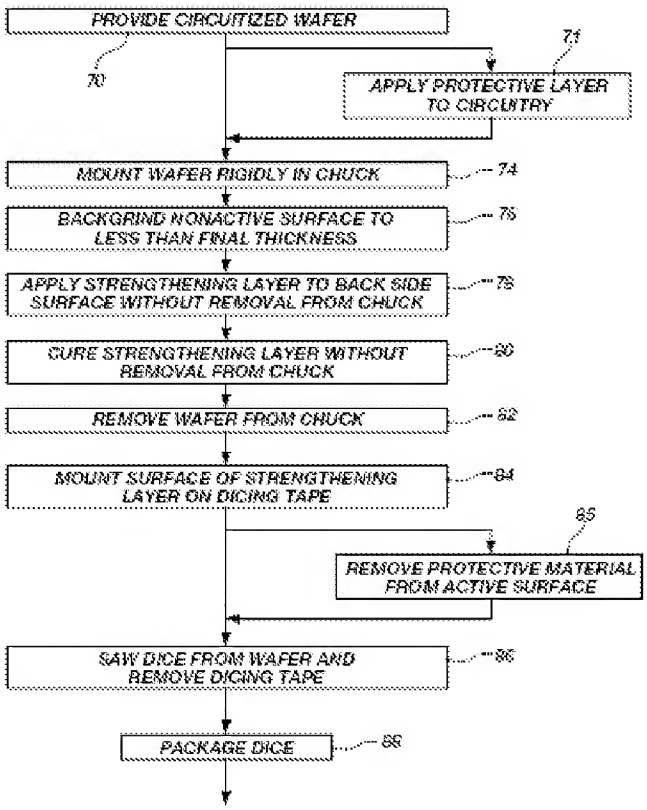

FIG. 9

MAILING ADDRESS OF SENDER (Please do not use customer number below):

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THE PATENT & TRADEMARK OFFICE MAILROOM DATE STAMPED HEREON IS AN ACKNOWLEDGEMENT THAT ON THIS DATE ') PATENT & TRADEMARK OFFICE RECEIVED

Transmittal Letter (2 pages, in duplicate); Part B - Issue Fee Transmittal (1 page); Check No. 21870 in the amount of $1,715.00; Amendment Pursuant to 37 C.F.R. § 1.312(a) (25 pages); Attached Replacement Sheet of Drawings (1 sheet) and Annotated Sheet Showing Changes Made (1 sheet); Comments on Statement of Reasons for Allowance (2 pages); and Fee Addressee for Receipt of PTO Notices Relating to Maintenance Fees (2 pages)

Invention:	THINNED, STRENGTHENED SEMICONDUCTOR SUBSTRATES
Applicant(s):	Derderian et al.
Filing Date:	October 21, 2003
Serial No.:	10/690,339
Date Sent:	June 30, 2005 via Express Mail Label EL 994849098 US
Docket No.:	2269-5713US
JAW/njj:sm	

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Derderian et al.

Serial No.: 10/690,339

Filed: October 21, 2003

For: THINNED, STRENGTHENED SEMICONDUCTOR SUBSTRATES

Confirmation No.: 2183

Examiner: D. Le

Group Art Unit: 2818

Attorney Docket No.: 2269-5713US (02-1473.00/US)

Notice of Allowance Mailed:

April 1, 2005

Express Mail Mailing Label No.: EL 994849098 US

Date of Deposit with USPS: June 30, 2005

Person making Deposit: Steve Wong

AMENDMENT PURSUANT TO 37 C.F.R. § 1.312(a)

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Please amend the above-referenced application as follows:

Amendments to the Title appear on page 3 of this paper.

Amendments to the Specification begin on page 4 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 20 of this paper.

Amendments to the Drawings appear on page 24 of this paper and include both an attached replacement sheet and an annotated sheet showing changes.

Remarks begin on page 25 of this paper.

An **Appendix** including amended drawing figures is attached following page 25 of this paper.

IN THE TITLE:

The title has been amended herein. Pursuant to 37 C.F.R. §§ 1.121 and 1.125 (as amended to date), please enter the title as amended.

THINNED, STRENGTHENED SEMICONDUCTOR SUBSTRATES AND PACKAGES INCLUDING SAME

IN THE SPECIFICATION:

Please amend paragraph number **[0002]** as follows:

[0002] State of the Art: The manufacture of semiconductor devices, commonly termed "dice" or "chips," encompasses a plurality of major manufacturing stages, each of which typically comprises a number of elements. In general, chip manufacture may be generalized as comprising the stages of crystal growth, wafer preparation, wafer fabrication, wafer sort, and packaging. Wafer sort and packaging may be performed in a different order, or combined into a single manufacturing stage. Typically, a wafer of a semiconductor ~~material~~ material, such as ~~silicon~~ silicon, is cut from a large crystal and may have a nominal diameter of up to about 300 mm (12 inches). Although larger bulk semiconductor substrates may have been fabricated, the 300 mm wafer is the largest size wafer currently being phased into commercial production runs by various semiconductor device manufacturers. As cut from a cylinder of semiconductor material transverse to the longitudinal axis thereof, a wafer typically has a thickness considerably greater than the usual end product of the semiconductor fabrication, i.e., singulated semiconductor dice.

Please amend paragraph number **[0003]** as follows:

[0003] A designated "active" surface of a bare wafer may be planarized, as by grinding and chemical-mechanical polishing (CMP) or etching (wet or dry) to a smoothness and planarity required for the formation of integrated circuits therein. A wafer 10 with a planarized active surface 12 and an unthinned ~~backside~~ back side surface 14 is shown in FIG. 2. The active surface 12 is shown as divided into a plurality of semiconductor dice 16 by "streets" 46. The bare ~~backside~~ back side surface 14 of the bare wafer 10 is shown in FIG. 3 as unthinned, unpolished and with a rough surface texture with "peaks" 24 and "valleys" 26 having a total amplitude 38 about a ~~backside~~ back side surface 14. As shown, the wafer 10 is to be thinned from an initial thickness 18 to a final thickness 22 at thinned ~~backside~~ back side surface 20. The wafer 10 has an overall nominal diameter 28 (FIG. 2) (but for the presence of a wafer flat, as is conventional).

Please amend paragraph number **[0006]** as follows:

[0006] The fabrication ~~stage~~ act 104 of IC production is concentrated on the "active" surface 12 of the wafer 10, which has undergone preliminary abrasive thinning and planarization/etching acts to planarize and smooth the active surface 12. The active surface 12 typically has a flatness value of about 3-4 μm as measured by the maximum peak-to-valley deviation of the wafer surface from a reference plane extending thereacross. A plurality of sets of identical integrated circuit patterns are simultaneously formed in discrete locations on the active surface 12 by a series of layer deposition and etching processes, as known in the art. The sets of circuit patterns are formed in rows wherein the rows of patterns are separated in X- and Y-axes by streets 46 free of circuitry. Electrical components such as transistors, resistors, capacitors and the like, as well as interconnecting conductors, i.e., "metallization" are typically formed in each pattern. When the active surface 12 of a wafer 10 is not planar (flat), as, for example, due to warping, the use of patterning ~~techniques~~ techniques, such as ~~photolithography~~ photolithography, to project a pattern onto the wafer surface results in distorted and out-of-specification image dimensions. Thus, a high degree of planarity is crucial to uniform high-yield production of semiconductor dice.

Please amend paragraph number **[0009]** as follows:

[0009] Thus, in current practice, upon completion of the fabrication acts 104, a protective coating or layer 48 (FIG. 4), in the form of a polymer layer or of a so-called "backgrind tape," is applied to the circuitized active surface 12 in act 106 to protect and support the circuitry during a bulk thinning, i.e., backgrinding act 110. The protective coating application is generally illustrated in FIG. 4 and various methods of the prior art are discussed, infra.

Please amend paragraph number **[0010]** as follows:

[0010] For the ~~thinning~~ backgrinding act 110, the active surface 12 with attached protective layer 48 is first mounted in a chuck (not shown) in act 108 to expose the ~~backside~~ back side surface 14 of wafer 10 for grinding. The backgrinding act 110 is performed to remove extraneous material from the wafer (thinning the wafer 10) from an initial thickness represented by ~~backside~~ back side surface 14 (see FIG. 4) to a desired thinned ~~backside~~ back side surface 20, at which point the wafer has a final thickness 22 (see FIG. 3). Typically, this material removal is conducted by a backgrinding act using an abrasive grinding pad or wheel 32 with abrasive particles 36 moved in one or more lateral directions 33 with respect to the plane of wafer 10 (see FIG. 4). Backgrinding generally leaves the ~~backside~~ back side surface 14 in a rough state, with a significant penetration of, and damage to, the crystal lattice (see FIG. 5). Lateral impact of the abrasive particles 36 against surface features in the form of peaks 24 with forces 34 cause further damage. Damage has been observed at depths of up to about 100 μm into the crystal lattice of a wafer 10. Thus, a further planarization act 112 is typically conducted to reduce ~~backside~~ back side surface damage from the backgrinding act 110.

Please amend paragraph number **[0011]** as follows:

[0011] Planarization approaches to reducing the ~~backside~~ back side surface damage due to rough grinding have generally been either to (a) perform a fine polishing by chemical-mechanical polishing (CMP) following backgrinding, or (b) plasma (dry) etch or (less commonly) wet etch the ~~backside~~ back side surface in act 112. These processes require the rough grinding to be halted prior to attaining the desired final thickness 22, so that the damaged zone of the crystal lattice will be removed in act 112. While these procedures smooth the ~~backside~~ back side surface 14 to reduce grinding damage, they have little or no beneficial effect upon warping tendencies. In fact, the additional thinning may enhance the proclivity of a wafer for warping. In the past, where wafer thicknesses as low as about 7-20 mils (about 180 - 500 μm) were considered adequate, the above-described processes worked relatively well. However, fine polishing and/or plasma-etching of ~~backside~~ back side surfaces of very thin wafers, i.e.,

having thicknesses of about 4 mils (about 100 μm) or even 2 mils (about 50 μm), is incapable of achieving the desired yield of dice free of unacceptable warping, cracking and even fracturing of the semiconductor material. The problem is greatly exacerbated by using wafers having larger diameters. For example, a wafer may require thinning from an initial thickness of 28 mils to a final thickness of 4 mils. In the thinned state, residual stresses (including backgrinding stresses) in the wafer tend to warp the wafer, a condition also known as "dishing," which is evident upon removal of a wafer from the chuck and/or upon removal of the protective ~~coating~~ layer 48 from the active surface 12. Damage due to backgrind thinning may lead to wafer fracture at the time of thinning (backgrinding act 110), upon release from the chuck in act 114, upon removal of a protective layer 48 from the active surface 12 in act 116, during attachment of a removable wafer dicing tape to the wafer in act 118, in die singulation in act 120, and in packaging ~~(act 122).~~ in act 122. Furthermore, while the rough grinding act is short (time-wise) and relatively inexpensive, the subsequent polishing or etch processes in act 112 are time-consuming and fairly expensive to conduct.

Please amend paragraph number **[0012]** as follows:

[0012] The role of the ~~backside~~ back side surface of the wafer, if any, is typically that of a mounting surface used to attach an individual semiconductor die to a carrier substrate of some sort. For example, the ~~backside~~ back side of a semiconductor die may be attached to a lead frame paddle, to an interposer, to a circuit board, to another die, or to some other substrate. In other instances, such as in the case of leads-over-chip packaging or in certain chip-scale packaging configurations, the ~~backside~~ back side of a semiconductor die may be encapsulated or merely coated. However, as package sizes have decreased, reduction in die (and thus wafer) thickness has been emphasized to reduce the thickness of the resulting packaged electronic device. Wafer thinning and planarization of the ~~backside~~ back side are required to reduce the wafer thickness to a desired dimension and provide a desired surface smoothness. The continual goal of producing integrated circuits of greater density (memory or logic components per unit volume) necessitates that semiconductor dice be of minimal thickness while retaining sufficient

resistance to breakage, warping, electrical degradation and dislocation formation. It is anticipated that reducing wafer thickness to the range of 2 mils or less will become commercially feasible in the near future, making the prevention of such damage even more difficult.

Please amend paragraph number **[0014]** as follows:

[0014] Conventional approaches to prevention of wafer damage during ~~backside~~ back side thinning and dicing have been largely concentrated on first providing a supportive protective layer 48 on the active surface to prevent damage to the circuitry. This act 106 is depicted in FIG. 4 and may be carried out in various configurations. For example, in U.S. Patent No. 5,476,566 to Cavasin, a double-sided tape is used to attach a support layer to the active surface. The tape and substrate may be removed prior to packaging by exposure to UV radiation.

Please amend paragraph number **[0015]** as follows:

[0015] In U.S. Patent No. 6,534,419 to Ong, electrical connection areas of the active surface are extended upwardly and a polymeric coating is applied to the active surface to cover the active surface. Backgrinding of the ~~backside~~ back side is then performed, followed by planarization of the active surface to expose the electrical connection areas.

Please amend paragraph number **[0019]** as follows:

[0019] Following application of a protective layer 48 over the active surface 12, the wafer 10 is clamped in a chuck (not shown) in act 108 for backgrinding and planarization in acts 110 and 112, already described. The wafer 10 is mounted to enable these acts to be readily accomplished on the ~~backside~~ back side surface 14. FIG. 5 depicts the rough ~~backside~~ back side surface 14 following grinding, and FIG. 6 depicts the ~~backside~~ back side surface 14 as being relatively planar following fine polishing in act 112.

Please amend paragraph number **[0020]** as follows:

[0020] Following polishing of the ~~backside~~ back side surface 14, the wafer 10 is removed from the chuck, and dicing tape 50 is attached to the ~~backside~~ back side surface 14 to enable singulation of wafer 10 without loss or misplacement of individual semiconductor dice 16 (see FIG. 7). This act 118 is well known in the art and may be performed either before or following the removal of protective layer 48 from the active surface 12.

Please amend paragraph number **[0023]** as follows:

[0023] In U.S. Patent No. 5,164,815 to Lim, cracking and delamination of the encapsulation layer of a semiconductor package due to high-temperature soldering is purportedly overcome by leaving the die ~~backside~~ back side as a rough surface to improve adhesion of the packaging material thereto. The invention pertains to packages of relatively high thickness, e.g., about 50 mils (1270 μm) and does not address warping of or damage to the wafer itself. The ~~backside~~ back side is roughened by a conventional backgrinding process.

Please amend paragraph number **[0024]** as follows:

[0024] In U.S. Patent No. 5,313,102 to Lim et al., cracking of the encapsulating layer of a semiconductor package due to subsequent exposure to high temperature is addressed by applying a coating of polyimide on the ~~backside~~ back side of the die prior to packaging. The polyimide is purported to enhance the adhesion of the encapsulation material and reduce cracking thereof. The invention again pertains to packages of high thickness, e.g., about 50 mils (1270 μm) and does not address warping of or damage to the wafer itself.

Please amend paragraph number **[0025]** as follows:

[0025] U.S. Patent No. 6,184,064 to Jiang et al. teaches the forming of a pattern of contours such as grooves, furrows, etc. in a wafer ~~backside~~ back side surface to enhance adhesion of an encapsulant or die attach adhesive thereto. The depth of the contours is preferably no greater than about 25 μm.

Please amend paragraph number **[0026]** as follows:

[0026] U.S. Patent No. 5,583,372 (hereinafter "the '372 patent") issued to King et al., assigned to the assignee of the present invention, discloses a semiconductor die including a metal layer deposited on the ~~backside~~ back side surface thereof for enhancing adhesion between the die and a molding compound, i.e., encapsulant compound. The metal layer is substantially oxide free and provides a uniform wetting surface for better adhesion. Furthermore, the '372 patent requires additional materials and fabrication processing, specifically depositing about 50 microinches of copper on the ~~backside~~ back side surface of the die and approximately 2-3 microinches of palladium over the copper layer.

Please amend paragraph number **[0028]** as follows:

[0028] In view of the foregoing discussion of the problems associated with conventional techniques for backgrinding wafers to an enhanced thinness, which problems are further exacerbated by increasing wafer diameter, it would be advantageous to form such extremely thin wafers while counteracting warping forces. It would also be advantageous to reduce the incidence of wafer fracture and breakage, to heal fracture, scratches and grooves which may occur, and to provide a planar ~~backside~~ back side surface on the wafer. It would be further desirable to complete the formation of a wafer of enhanced thinness in a configuration which prevents subsequent propagation of lattice defects during die singulation, testing, packaging, attachment to a substrate, and end use. It would also be desirable to enhance the attachment of packaging materials to the ~~backside~~ back side of a die and to provide an ionic barrier over the wafer ~~backside~~ back side surface.

Please amend paragraph number **[0029]** as follows:

[0029] The present invention, in an exemplary embodiment, comprises a method for producing a very thin substrate while eliminating or minimizing breakage, cracking and warping thereof at the bulk, or wafer, stage and thereafter. In the method of the present invention, a

semiconductor substrate, for example, in the form of a wafer is mounted in a chuck for ~~backside~~ back side processing. The ~~backside~~ back side of the wafer is background to thin the wafer without significant polishing thereof. A reinforcement layer or film of highly penetrating hardenable material is then applied to the rough surface of the ~~backside~~ back side while the wafer continues to be supported in an unwarped condition. The applied layer or film is cured to fill in valleys or vugs, micro-fractures, scratches and grooves in the ~~backside~~ back side surface. The applied layer forms a smooth, generally planar surface over the rough topography of the ~~backside.~~ back side. The applied layer is then hardened to a solid state before being released from the chuck. The hardened layer or film is tenaciously adhered to the ~~backside~~ back side and simultaneously counteracts forces tending to warp the wafer, heals defects in the ~~backside~~ back side surface and prevents warping, fracture or other damage to the ~~backside~~ back side surface during singulation of semiconductor dice from the wafer and subsequent packaging or attachment to a carrier substrate. The hardened reinforcement layer or film remains on each singulated semiconductor die and becomes part of its packaging or of an assembly of which it is a component. The reinforcement layer or film provides a planar ~~backside~~ back side surface for attachment to a carrier substrate, and the material of the reinforcement layer may be selected for compatibility with and adherence to a dielectric material used to encapsulate the die. Due to the presence of the reinforcement layer or film, the semiconductor dice cut from the wafer are maintained in an improved state of planarity and structural integrity to resist warping and mechanical damage. The surface roughness present at the conclusion of the backgrind operation enhances attachment of the reinforcement layer or film to the wafer ~~backside~~ back side surface. Thus, a thinning method ~~which~~ that leaves the ~~backside~~ back side surface in a state of micro-roughness is preferred. A fine polishing act is not required and, in fact, is not desirable.

Please amend paragraph number **[0030]** as follows:

[0030] The reinforcement material may comprise, for example, a polymer of any of the groups of epoxies or acrylics or, more particularly, a thermal or ultraviolet (UV) cross-linkable polymer, or a two-part epoxy. Other classes of coatings which may be used include, without

limitation, silicones, urethanes and siloxanes. Preferably, the reinforcement material, when hardened, forms a layer which is bonded securely to the wafer ~~backside~~ back side surface, resists internal bending stresses within the wafer material, has a coefficient of thermal expansion (CTE) similar to, and desirably slightly greater than, that of the wafer material, is resistant to cracking, has a substantially planar exposed surface, and is easily applied. The relatively coarse nature of the bare ~~backside~~ back side after grinding enhances the penetration and adhesion of the reinforcement layer or film. Use of a reinforcement material with a slightly greater CTE than that of a substrate material, such as silicon, will place the substrate material in a beneficial state of compression, resulting in a more robust structure.

Please amend paragraph number **[0031]** as follows:

[0031] The selected method for applying the reinforcement material to the bare substrate surface may be any method which will produce a relatively planar surface. For example, the coating method may comprise dispensing, screen-coating, stencil-coating, or spin-coating of a flowable material. Alternatively, the reinforcement material may be formed as a solid element, laminated to the substrate surface and bonded thereto. The reinforcement material may be a tape or film element ~~which is~~ applied to the substrate, heated to a flowable state to bond to the substrate and provide a substantially planar, exposed surface, and cooled to solidify. Other application methods include chemical vapor deposition (CVD) or plasma-enhanced chemical vapor deposition (PECVD). A Parylene™ deposition process may also be used, in which a dimer is vaporized to a monomer and exposed at lower temperatures to a surface, depositing a tenacious polymer on the surface. An exemplary dimer used in the Parylene™ process is di-para-xylene.

Please amend paragraph number **[0033]** as follows:

[0033] The advantages of the present invention include the fabrication of a wafer in which warping stresses are counteracted during manufacture and subsequent use of individual semiconductor dice singulated therefrom, wafer ~~backside~~ back side surface damage due to

backgrinding is repaired, very thin wafers of large diameter may be effectively produced at a high yield rate, and polishing of the thinned wafer ~~backside~~ back side is not required, thus saving substantial time and expense. Furthermore, the layer or film of reinforcement material of the present invention may be used to counteract stresses on the wafer induced by the presence of a protective layer applied over the active surface prior to thinning. Still further, the layer or film of reinforcement material may be applied using well-developed process technologies. In addition, the applied layer or film of reinforcement material remains as a part of the finished semiconductor die and may be used to enhance adhesive attachment of the die to a packaging material or carrier and provide an ionic barrier.

Please amend paragraph number **[0042]** as follows:

[0042] FIG. 7 is an enlarged cross-sectional side view of a portion of a semiconductor wafer following removal of a protective layer from the active surface and application of a dicing tape to the ~~backside~~ back side according to the prior art;

Please amend paragraph number **[0046]** as follows:

[0046] FIG. 11 is an enlarged cross-sectional side view of a portion of a semiconductor wafer following application and hardening of a reinforcement layer or film to the ~~backside~~ back side surface thereof according to the present invention;

Please amend paragraph number **[0047]** as follows:

[0047] FIG. 12 is an enlarged cross-sectional side view of a portion of a semiconductor wafer following application of dicing tape to the ~~backside~~ back side surface thereof according to a method of the present invention; and

Please amend paragraph number **[0050]** as follows:

[0050] In act 74, the wafer 10 is clamped into a fixture, for example, in the form of chuck 60 (see FIG. 10) such that the ~~backside~~ back side surface 14 is exposed for backgrinding

in subsequent act 76. The chuck 60 that is used must be capable of holding and maintaining the wafer 10 in a planar configuration in spite of increasing warping tendencies that may be induced or magnified during grinding. Various wafer chucks 60 in the art are suitable for use. Especially applicable are those which rigidly grip the wafer edge (i.e., edge bead ring EBR) 58 (FIG. 10) about the circumference, maintaining the wafer in a nonwarping configuration. Another example of a chuck that may be used is described in U.S. Patent No. 6,279,976 to Ball, assigned to the assignee of the present application, and hereby incorporated herein by reference thereto. This chuck holds a wafer against a planar backing structure by vacuum.

Please amend paragraph number **[0051]** as follows:

[0051] In act 76, illustrated in FIG. 10, the ~~backside~~ back side surface 14 is rough-ground to a level at which the mean wafer thickness 23 between the active surface 12 and the rough ~~backside~~ back side 14 is less than the desired final ~~mean~~ wafer thickness 22 (indicated in broken lines at thinned back side surface 20). The method chosen to backgrind may be a physical abrasive process, e.g., with an abrasive pad or wheel, CMP or other method which will quickly and effectively thin the wafer 10 and provide a rough, unpolished ~~backside~~ back side surface 14. Fine polishing is neither necessary nor desirable. It is preferred that the backgrinding effectively remove material to a level below the desired final ~~mean~~ wafer thickness 22, which is desirably less than about 10 mils. More preferably, the back-ground mean wafer ~~mean~~ thickness 23 is less than about 5 mils, and thicknesses as low as 3 mils or less, i.e., 2 mils or 1 mil, may also be achieved. The backgrind leaves the ~~backside~~ back side surface 14 with a surface roughness factor R_a which is generally between about 5% and about 40% of the mean thickness of the ~~backside~~ back side ground wafer 10. Expressed another way, the surface roughness factor R_a is between about 2 μm and about 15 μm for wafers 10 as thin as about 2 mils or less (about 51 μm). An additional fine-grinding act may be performed only in the event that the rough backgrinding leaves the ~~backside~~ back side surface in an excessively rough state.

Please amend paragraph number **[0053]** as follows:

[0053] Continuing with FIG. 9, the next act 78 is to apply a layer 40 of a reinforcement material to the rough ~~backside~~ back side surface 14. The reinforcement layer 40 is applied without removing the wafer 10 from its rigid position in chuck 60, thus maintaining the wafer 10 in an unwarped configuration. In general, the reinforcement layer 40 is formed over rough ~~backside~~ back side surface 14 to exhibit a substantially planar, level ~~backside~~ thinned back side surface 20. The reinforcement layer 40 fills recesses in the topography (valleys 26 between peaks 24) of ~~backside~~ back side surface 14 and preferably overcovers the peaks 24 to at least a very minimal degree. In general, it is desirable to use the thinnest reinforcement layer 40 ~~which~~ that will achieve the desired antiwarping effect so as to leave as much of the substrate material intact while still achieving a desired thinness. Thus, the reinforcement layer 40, at a minimum, covers the highest peaks 24 of the rough ~~backside~~ back side topography, but may be of greater thickness thereover, such as an additional 100 μm or more. Preferably, the additional layer thickness above the peaks 24 is up to about 10 μm.

Please amend paragraph number **[0054]** as follows:

[0054] The reinforcement material may desirably comprise any material which has the following qualities:

(a) it may be bonded securely to the ~~backside~~ back side surface and hardened to form a strong, rigid, permanent support for the substrate material for maintaining the wafer in an unwarped state when released from the grinding chuck and subjected to subsequent processing and handling;

(b) it readily and substantially completely penetrates grooves, cracks and other vugs in the ~~backside~~ back side surface of the wafer;

(c) it exhibits a coefficient of thermal expansion (CTE) ~~which is~~ substantially similar to, and preferably slightly greater than, the CTE of the semiconductor material of the wafer, minimizing any CTE mismatch which would induce wafer warpage due to temperature

variations experienced during processing and subsequent operation while placing the semiconductor material in a beneficial state of compression; and

(d) it readily forms a relatively planar external surface when hardened.

Further, although this is not a requirement of the invention, it is normally desirable that the material of the reinforcement layer be a dielectric material.

Please amend paragraph number **[0055]** as follows:

[0055] Materials from which the reinforcement layer 40 may be formed include various polymers such as, for example, without limitation, epoxies, acrylics, silicones, urethanes, siloxanes, and Parylenes™. Thus, for example, the reinforcement layer 40 may be applied as a liquid polymer by application methods known in the art which will produce a relatively planar surface. For example, the coating method may comprise simple dispensing, screen-coating, stencil-coating, or spin-coating of a flowable material. The reinforcement material may be a thermoset cross-linkable polymer or a UV-stimulated cross-linkable polymer, commonly termed a "photopolymer." In another variation, an epoxy material can be cured to a so-called "B" stage of tackiness, at which it is still flowable. The epoxy material may then be applied to the ~~backside~~ back side surface 14 and reheated to complete the cure, bond to the surface and harden. It is contemplated that a layer of epoxy material may be applied to a backing sheet carrying a release layer, cured to a "B" stage and applied to the ~~backside~~ back side surface 14. The backing may then be stripped off, and the epoxy cure and hardening completed.

Please amend paragraph number **[0057]** as follows:

[0057] In a deposition method of newer development, the Parylene™ deposition process may be used. In this method, an organic dimer is heated to form monomers and then applied at a lower temperature to a ~~backside~~ back side surface 14 where it deposits as a polymeric reinforcement layer 40. A dimer such as di-para-xylene may be used.

Please amend paragraph number **[0058]** as follows:

[0058] Another deposition method which may be used comprises the formation of a tape or film element of partially polymerized material. The tape or film may then be applied to the ~~backside~~ back side surface 14, heated to flow, bond to the surface, level and planarize, and finally cooled to a solid state.

Please amend paragraph number **[0059]** as follows:

[0059] In act 80, the polymer reinforcement layer 40 may be subjected to a final cure, typically by a thermal, UV radiation or other means known in the art, while the chuck 60 continues to hold and support the wafer 10 in a rigid, nonwarping condition. The term "cure" is used herein in its broadest context, indicating only that a reinforcement material applied to a ~~backside~~ back side surface 14 of a wafer 10 solidifies and bonds thereto. The resulting wafer 10 is depicted in FIG. 11 with a desired final thickness 22 between the active surface 12 and the final ~~backside~~ thinned back side surface 20.

Please amend paragraph number **[0060]** as follows:

[0060] In act 82, the wafer with reinforcement layer 40 is removed from the chuck 60. Of general prior art practice, a dicing tape 50 is attached to the final ~~backside~~ thinned back side surface 20 (act 84) as seen in FIG. 12, and individual semiconductor dice 16 (FIG. 1) are singulated by cutting along the streets (cut lines) 46 (in act 86). In a final act 88, a package 30 (see FIG. 13) is typically formed by encapsulating the singulated semiconductor dice 16 with a silicon-filled polymer encapsulant 52 and having (by way of example only) electrical terminals 54 on conductive pads 56 extending therethrough for connection to a substrate. The reinforcement layer 40 remains on the semiconductor die 16 and becomes part of the protective packaging, retaining its resistance to any warpage-inducing stresses resident within the substrate of the semiconductor die 16. The reinforcement layer 40 may be formulated to also provide a high-adhesion surface for encapsulant 52 applied over the covered ~~backside~~ back side surface 14

and prevents foreign matter from grinding from collecting within the encapsulant 52 and causing fracture of the hardened encapsulant 52.

Please amend paragraph number **[0061]** as follows:

[0061] Suitable materials for reinforcement layer include, without limitation: Ablebond 2025 thermally curable nonconductive die attach adhesive Ableflex 6200 B-stageable nonconductive adhesive from Ablestik Laboratories of Rancho Dominguez, California; T693/R3001 thermally curable nonconductive adhesive from Nagase Chemtex Corporation of Osaka, Japan; and #5031 wafer ~~backside~~ back side tape from Lintec Corporation of Tokyo, Japan.

Please amend paragraph number **[0062]** as follows:

[0062] Returning now to FIG. 9, another variation of the instant invention is also indicated. Thus, before mounting the wafer 10 in a chuck 60 (act 74) for backgrinding (act 76), a protective layer 48 is formed or applied in act 71 over the circuitry on the active surface 12. This act 71 may be taken to avoid or reduce any damage to the circuitry by pressure thereof against the clamping chuck 60. The protective layer 48 is illustrated as part of the prior art in FIGS. ~~4, 5, and 6~~ 4-6 and may be applied to the inventive method as well. The protective layer 48 is shown as removed in act 85 prior to dicing of the wafer 10.

Please amend paragraph number **[0064]** as follows:

[0064] The invention is applicable to semiconductor wafers formed from any thinnable material with a tendency to fracture and/or warp when thinned to a desired thickness value. Thus, it may be used for the ~~backside~~ back side thinning of, for example, silicon, gallium arsenide, germanium and indium phosphide materials, as well with substrates of other semiconductor materials. The method may be used for thinning nonsemiconductor materials, such as quartz and glasses, as well.

Please amend paragraph number **[0065]** as follows:

[0065] Although the foregoing description contains many specifics, these should not be construed as limiting the scope of the present invention, but merely as providing illustrations of some of the presently preferred embodiments. Similarly, other embodiments of the invention may be devised which do not depart from the spirit or scope of the present invention. Moreover, features from different embodiments of the invention may be employed in combination. The scope of the invention is, therefore, indicated and limited only by the appended claims and their legal equivalents, rather than by the foregoing description. All additions, deletions, and modifications to the invention, as disclosed herein, which fall within the meaning and scope of the ~~claims~~ claims, are to be embraced thereby.

IN THE CLAIMS:

Claims 1 – 26 and 50 – 52 were previously cancelled. Claims 27, 34, 35 and 43 have been amended herein. All of the pending claims are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

Listing of Claims:

1.-26. (Cancelled)

27. (Currently amended) A semiconductor wafer having an active surface and a ~~backside~~ back side surface and including a plurality of semiconductor dice formed thereon, wherein:

the active surface includes integrated circuitry thereon;

the ~~backside~~ back side surface is in a back-ground state;

a solid material extends over and is bonded to the ~~backside~~ back side surface; and

an interface between the ~~backside~~ back side surface and the solid material has a mean surface roughness factor R_a of between about 5% and about 40% of a mean thickness of the semiconductor wafer.

28. (Original) The semiconductor wafer of claim 27, wherein semiconductor material of the semiconductor wafer comprises one of silicon, gallium arsenide, germanium and indium phosphide.

29. (Original) The semiconductor wafer of claim 27, wherein the interface has a mean surface roughness factor R_a between about 2 μm and about 15 μm.

30. (Original) The semiconductor wafer of claim 27, wherein the solid material comprises a polymer.

31. (Original) The semiconductor wafer of claim 27, wherein the solid material includes at least one of the polymer groups comprising epoxies, acrylics, silicones, urethanes, siloxanes and Parylenes™.

32. (Original) The semiconductor wafer of claim 27, wherein the solid material comprises one of a thermoset cross-linkable polymer, a UV cross-linkable polymer and a two-part epoxy.

33. (Original) The semiconductor wafer of claim 27, wherein the solid material comprises a Parylene™ polymer.

34. (Currently amended) The semiconductor wafer of claim 27, wherein the solid material has a mean thickness of about 100 μm or less over a highest topographic feature on the ~~backside~~ back side surface.

35. (Currently amended) The semiconductor wafer of claim 27, wherein the solid material has a mean thickness of about 10 μm or less over a highest topographic feature on the ~~backside~~ back side surface.

36. (Original) The semiconductor wafer of claim 27, wherein the solid material has a generally planar exposed surface.

37. (Original) The semiconductor wafer of claim 27, wherein the solid material comprises an ionic barrier.

38. (Original) The semiconductor wafer of claim 27, wherein the semiconductor wafer has a thickness of about 4 mils or less.

39. (Original) The semiconductor wafer of claim 27, wherein the semiconductor wafer has a thickness of about 2 mils or less.

40. (Original) The semiconductor wafer of claim 27, wherein the semiconductor wafer has a nominal diameter of at least about 200 mm (about 8 inches).

41. (Original) The semiconductor wafer of claim 27, wherein the semiconductor wafer has a nominal diameter of at least about 300 mm (about 12 inches).

42. (Original) The semiconductor wafer of claim 27, wherein material of the semiconductor wafer is in a state of compression.

43. (Currently amended) A semiconductor package, comprising:

a die of semiconductor material having an active surface and a ~~backside~~ back side surface;

integrated circuitry on the active surface;

wherein the ~~backside~~ back side surface is in a roughly back-ground state and includes a solid material extending thereover and bonded thereto;

a protective material encapsulating at least a portion of the die and the solid material extending over the ~~backside~~ back side surface; and

a plurality of conductive terminals exposed through the protective material on a surface of the package;

wherein an interface between the ~~backside~~ back side surface and the solid material has a mean surface roughness factor R_a of between about 5% and about 40% of the mean thickness of the die.

44. (Original) The package of claim 43, wherein the interface has a mean surface roughness factor R_a of between about 2 μm and about 15 μm.

45. (Original) The package of claim 43, wherein the solid material comprises a polymer.

46. (Original) The package of claim 43, wherein the solid material includes at least one of the polymer groups comprising epoxies, acrylics, silicones, urethanes, siloxanes and Parylenes™.

47. (Original) The package of claim 43, wherein the solid material comprises one of a thermoset cross-linkable polymer, a UV cross-linkable polymer and a two-part epoxy.

48. (Original) The package of claim 43, wherein the solid material comprises a Parylene™ polymer.

49. (Original) The package of claim 43, wherein the semiconductor material of the die is in a state of compression.

50.-52. (Cancelled)

IN THE DRAWINGS:

The attached sheet of drawings includes a change to FIG. 9. This sheet replaces the original sheet including FIG. 9.

Specifically, FIG. 9 has been revised to change the first line of the label within the box identified by reference numeral --78-- from "APPLY STRENGTHENING LAYER TO BACKSIDE" to --APPLY STRENGTHENING LAYER TO BACK SIDE--. No new matter has been added.

REMARKS

This amendment corrects errors in the text and drawings. Entry is respectfully solicited.

This amendment is submitted prior to or concurrently with the payment of the issue fee and, therefore, no petition or fee is required. No new matter has been added.

Respectfully submitted,

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Date: June 30, 2005
JAW/csw

Enclosures: Replacement Sheet
Annotated Sheet Showing Changes

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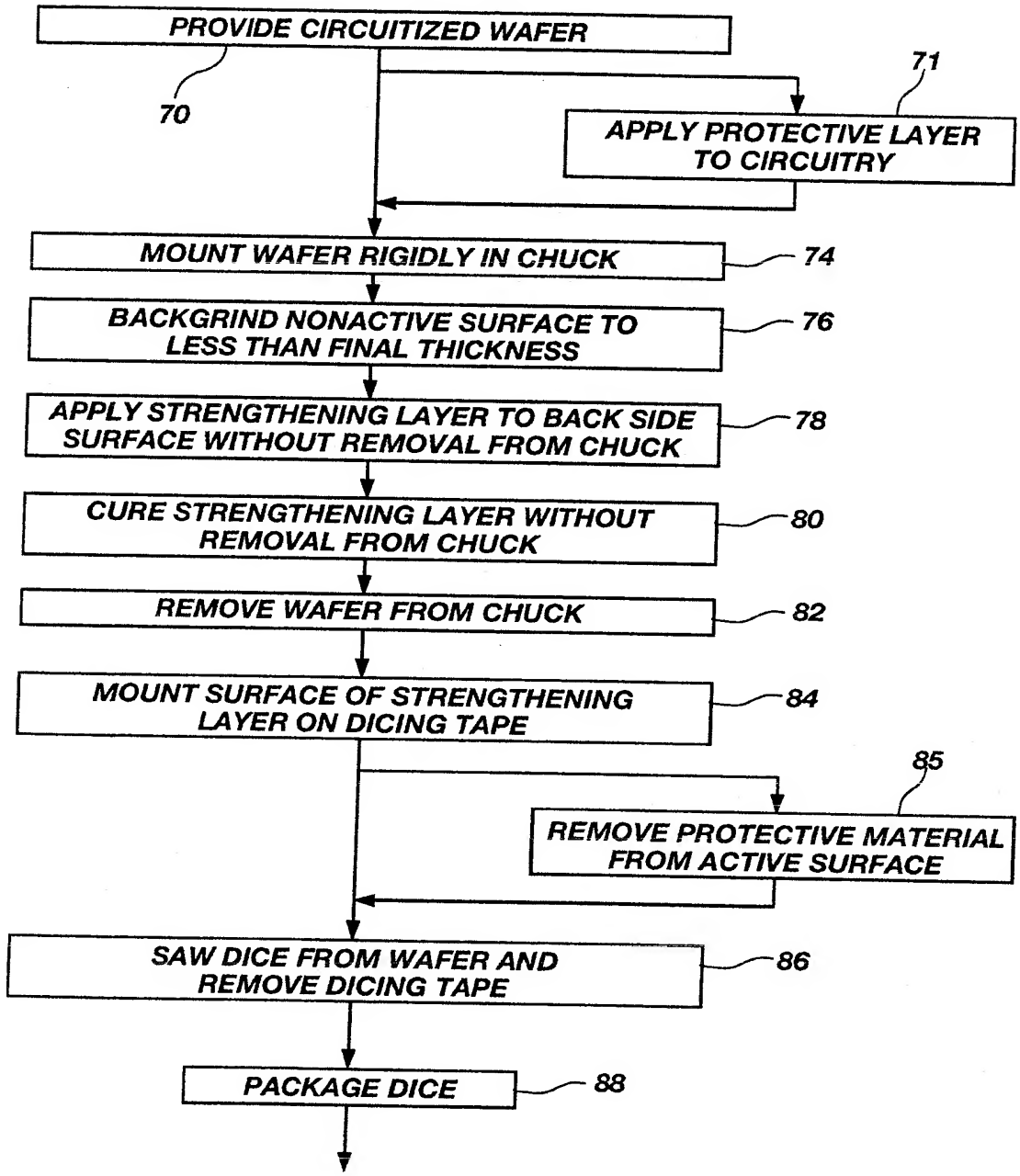
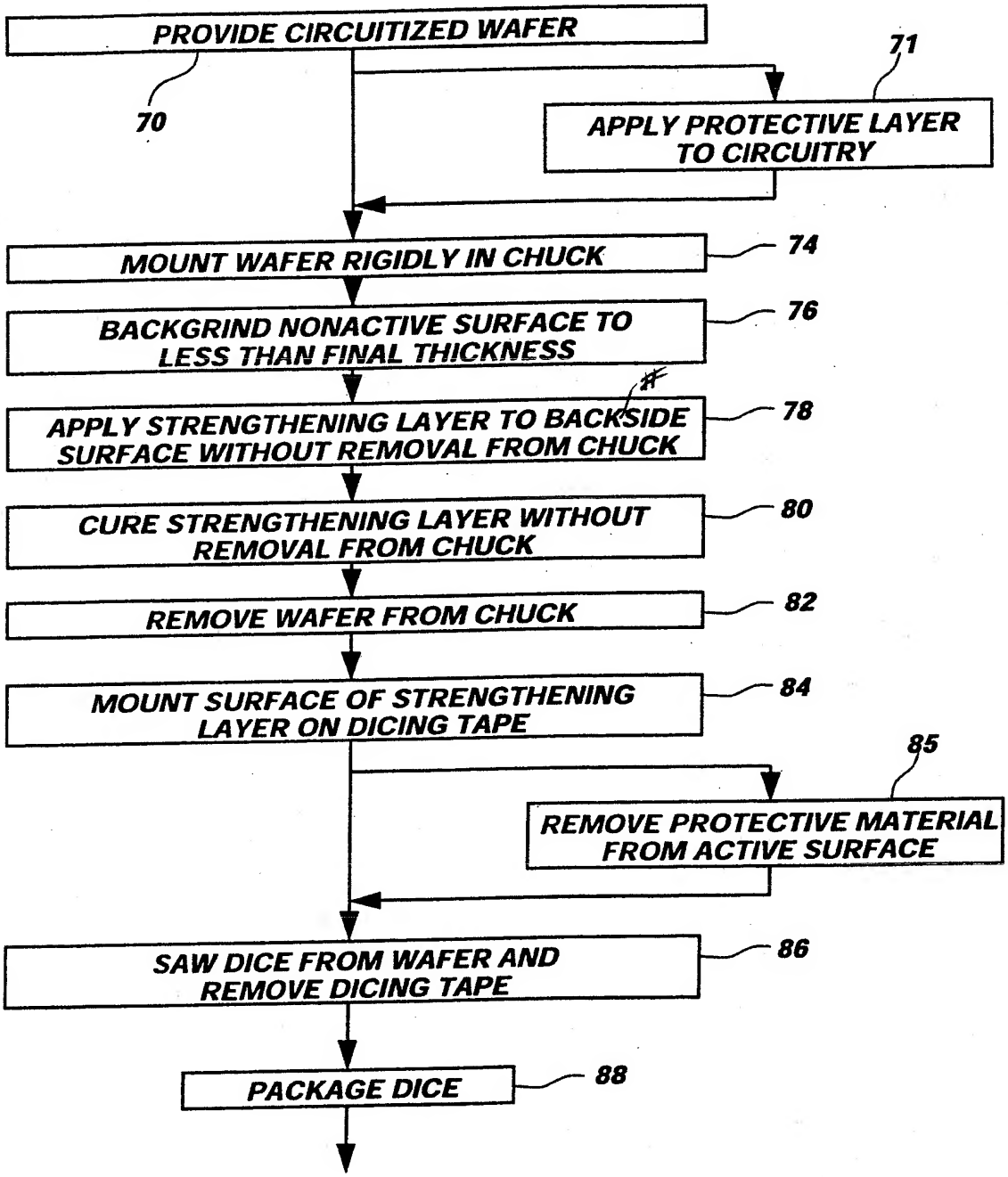

PROVIDE CIRCUITIZED WAFER
70
71
APPLY PROTECTIVE LAYER TO CIRCUITRY
MOUNT WAFER RIGIDLY IN CHUCK
74
BACKGRIND NONACTIVE SURFACE TO LESS THAN FINAL THICKNESS
76
APPLY STRENGTHENING LAYER TO BACK SIDE SURFACE WITHOUT REMOVAL FROM CHUCK
78
CURE STRENGTHENING LAYER WITHOUT REMOVAL FROM CHUCK
80
REMOVE WAFER FROM CHUCK
82
MOUNT SURFACE OF STRENGTHENING LAYER ON DICING TAPE
84
85
REMOVE PROTECTIVE MATERIAL FROM ACTIVE SURFACE
SAW DICE FROM WAFER AND REMOVE DICING TAPE
86
PACKAGE DICE
88

FIG. 9


PROVIDE CIRCUITIZED WAFER
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APPLY PROTECTIVE LAYER TO CIRCUITRY
MOUNT WAFER RIGIDLY IN CHUCK
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76
APPLY STRENGTHENING LAYER TO BACKSIDE SURFACE WITHOUT REMOVAL FROM CHUCK
78
CURE STRENGTHENING LAYER WITHOUT REMOVAL FROM CHUCK
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REMOVE WAFER FROM CHUCK
82
MOUNT SURFACE OF STRENGTHENING LAYER ON DICING TAPE
84
85
REMOVE PROTECTIVE MATERIAL FROM ACTIVE SURFACE
SAW DICE FROM WAFER AND REMOVE DICING TAPE
86
PACKAGE DICE
88

FIG. 9